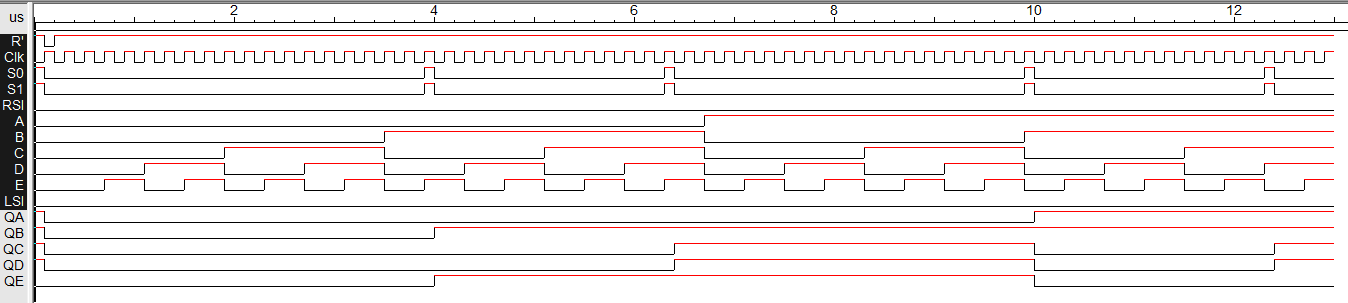
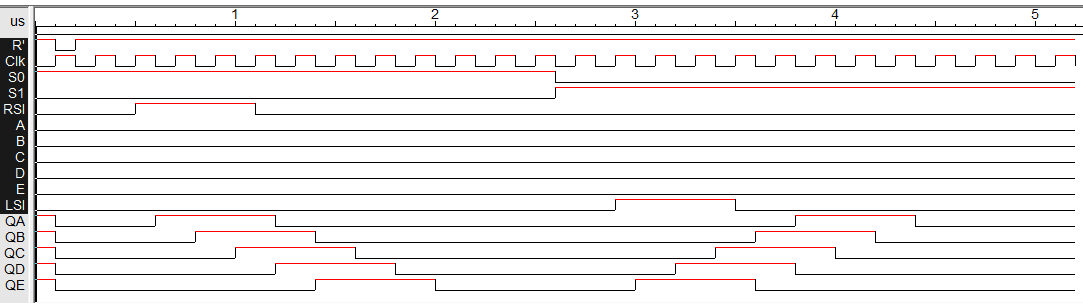
**Assignment # 3**

**Question 1**

**Results for part b**

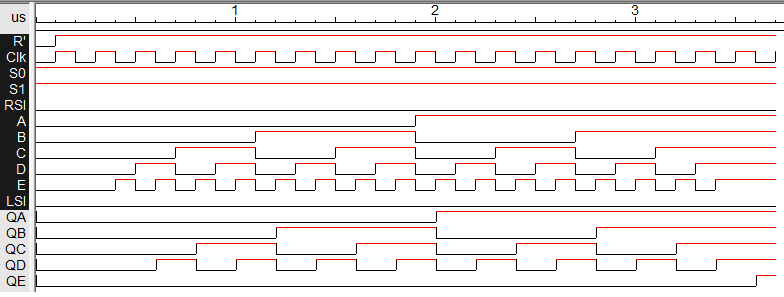
First I set S0 and S1 to 0, and entered random values for the inputs A, B, C, D and E to see if the outputs would hold. Below is the result:

You can see that the output values hold. (Note: I changed S1 and S0 to 1 at certain points so it can load new values, and then back to hold mode so that is shows that the circuit can hold the new values)

Then I to test the Shifting properties of the circuit, I first let S0=1 and S1=0 and then vice versa. The patterns of the output show the effect of shifting right and then left. Below is the result:

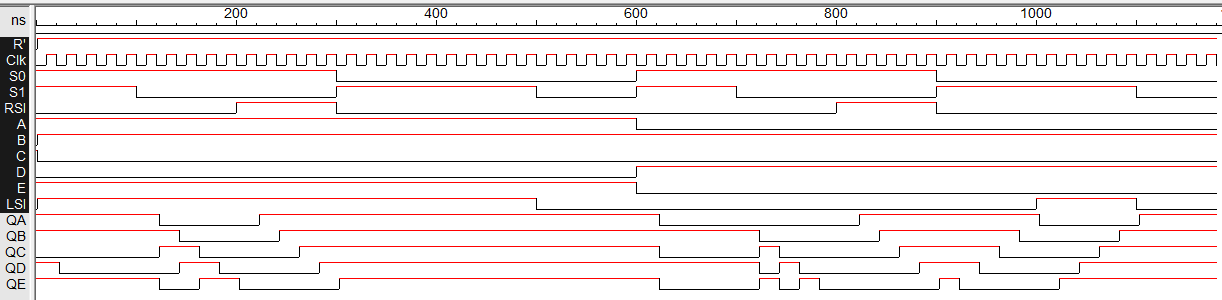
When S0 = 1, you can see the outputs shifting right, starting from RSI=1 and when S1=1 and LSI=1, you can see the outputs shift left.

Finally, I set S0 and S1 = 1, and tried random values for the Inputs A, B, C, D and E to test if the circuit would load new values. Below is the result:



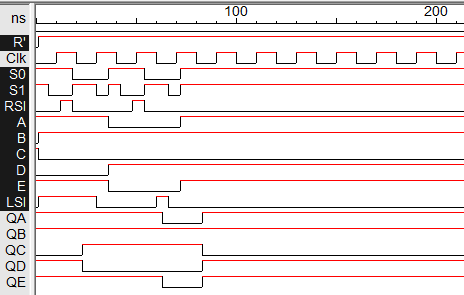
We can see that new values are being loaded (also demonstrated in the hold test). All the four tests show that the circuit is functioning as a 5 bit shift register.

**Results for part c**

I tested another time file which showed all four cases in one run. Below is the result at max frequency:

We can see all the aspects of the shift register here. This is the output at max frequency.

For Part c, my maximum frequency was 142.87 MHz. this translates to 1/7 ns. So in order to test the file for a frequency bigger than max frequency, I used 1/6 ns. This was the following result:



If we compare the results for the analysis at max frequency and the one at 1/6 ns, or 166.67 MHz, we can notice a huge difference. That tells us that the circuit does not operate at a frequency bigger than max frequency.